ADVANCED FUEL RESEARCH
P. O. Box 380379
East Hartford, Connecticut 06138-0379
Telephone (203) 528-9806
Fax (203) 528-0648

PHASE I
MONTHLY PROGRESS REPORT

Advanced Fuel Research, Inc.
87 Church Street
East Hartford, CT 06108

Navy Contract No: N00014-94-C-0261

"HTS Josephson Technology on Silicon with Application to High Speed Digital Microelectronics"

Report Sent:
Report No.: (0001AG)
Report Period: April 1 - April 30, 1995
Contract Period: September 30, 1994 - September 29, 1995

Prepared By:
Peter A. Rosenthal, Principal Investigator
and Joseph E. Cosgrove
Advanced Fuel Research, Inc.

and

Professor Michael Guvvitch, Professor Sevgey Tolpygo,
Professor K.K. Likhavev
Boris Nadgorny & Sergey Shokhor

Original contains color plates: All DTIC reproductions will be in black and white

for

Office of Naval Research, Arlington, VA
AFR Project No.: 531001

UNCLASSIFIED

May 4, 1995

In this months report, are pleased to report what we consider to be a significant breakthrough, and an important program milestone. **The Stony Brook group successfully fabricated and demonstrated correct operation of an HTS RSFQ flip-flop, fabricated on a lanthanum aluminate substrate.** To our knowledge, this is the first unequivocal demonstration of a working multijunction RSFQ digital element fabricated from HTS thin films. This work is reported below under the Task 3 heading. In addition to the RSFQ demonstration, we convened a meeting at Stony Brook to review the first six months of the program and to refine our plans for the second half of the program. The conclusions of the meeting are summarized below.

Phase I Accomplishments -

- Working josephson junctions and SQUIDs have been fabricated on silicon substrates. The electrical properties are similar to those fabricated on more conventional substrates such as $LaAlO_3$.
- **A YBCO RSFQ rs flip flop with I/O test structures was successfully designed, fabricated and tested.**
- The kinetic inductance and London penetration depth of the films on silicon have been determined from measurements of HTS SQUIDs on silicon.
- An approach to alleviating film stress due to thermal expansion coefficient mismatch has been outlined. The proposed solution involves fabricating a functionally graded buffer layer that flows plastically to relieve film stress while at the same time, allows nucleation and growth of heteroepitaxial films.

Remaining Hurdles for the Phase I program -

- Film uniformity and process throughput must be improved to improve device uniformity and yield on silicon substrates. Multiple junctions with similar critical temperatures and critical currents must be demonstrated on a single chip.
- RSFQ elements must be fabricated on silicon substrates. When the device reproducibility has been judged adequate, we will attempt to fabricate the rs flip-flop on silicon.
- RSFQ elements on silicon must be tested and analyzed.

Other activities:

Task 1:Junction fabrication and testing

Improvements to the PLD system -
To improve film quality and throughput, a new substrate heater was designed and constructed for the AFR PLD facilty. The new furnance heats the substrates with improved uniformity, and it handles larger (12 mm square) substrates. The larger substrates can be diced into four 5 mm substrates at Stony Brook, allowing a fourfold increase in process throughput. This is particularly important because a good film now offers four chances for device fabrication.

Task 2: Junction modeling - No activities on Task 2.

Task 3: RSFQ device fabrication

A working RSFQ circuit with 14 junctions was successfully fabricated and tested, using a YBCO film grown on a lanthanum aluminate ($LaAlO_3$) substrate. This result is significant because it demonstrates that:
1) the junction technology is sufficiently controllable to manufacture circuits with a significant number of junctions (14 junctions),
2) The circuit design was correct and the film and junction properties e.g. kinetic inductance and critical currents, were within the specified operating margins for successful circuit operation.
3) Correct pulse driven RSFQ logic operation can be successfully verified through dc testing.

Following, find a brief report of these activities, supplied by Professor Michael Gurvitch and his co-workers at Stony Brook.

INTRODUCTION

Direct e-beam writing technique (DEW) was used for preparation of an RSFQ RS Flip-Flop on YBCO thin film operating at 26 K.

The most important unique features of the DEW technique instrumental for successful operation of RSFQ circuits are:

1) tunability of the critical temperature T_c (and hence the critical current I_c at an operating temperature)

2) simplicity of the in-plane two-dimentional design combined with the freedom in the arrangement of the junctions.

TECHNOLOGY

Layout of the circuit under investigation is shown in Fig. 1. It was made of 500 Å YBCO film deposited on $LaAlO_3$ at AT@T Bell Labs by Shang Hou. After the deposition the wafer was diced into 5x5 mm chips, which were then used for patterning. The patterning was done by standard optical lithography with PMMA resist. YBCO film was wet-etched in diluted HNO_3. Fig. 2 shows the final pattern with the minimal feature of 2 μm. Then the junctions were made by DEW in the places shown in Fig. 1 as straight lines across the bridges. Electron beam of CM-12 Philips Electron Microscope was scanned once across a bridge to form a week link. The parameters of the beam were as follows: energy E=120 keV, probe size 35 Å, beam current 5 nA. T_c of the junctions after writing was approximately 35 K.

OPERATION OF THE RSFQ RS Flip-Flop.

Fig. 3 shows the equivalent circuit of the RS Flip-Flop used in the experiment. Below we give a brief description of how it works and then demonstrate its operation at 26 K.

The circuit has a left-right symmetry and consists of four main parts (see Fig. 1 and 3).

1. **DC/SFQ converter** (J1, J2). Current IL opens J2. As a result the fluxoid starts moving to the right by the driving current I2 and antifluxoid to the left. The latter is trapped in the first hole and then comes out of the circuit through J1 when IL is decreased.

2. **Transmission line**. The fluxoid keeps moving along the transmission line through the junctions J3 and J4 by the driving currents I3 and I4.

3. **RS Flip-Flop**. (The main cell of the device). Finally the fluxoid gets into the loop J6L, J6R and stays there in the absence of a driving force.

4. **SFQ/DC converter** (J7L and J7R). It serves as an output of the Flip-Flop. It detects the flux in the lower loop cell . State "1" corresponds to the state when one fluxoid is

trapped in the lower loop which results in the corresponding voltage in the upper SQUID when it is biased by some current higher than its critical current. State "0" corresponds to the absence of a fluxoid in the lower cell. This is achieved by applying current IR to the right part of the device. It generates an antifluxoid which moves to the left and annihilates with the previously trapped fluxoid in the main cell. If IL generates the fluxoid and the Flip-Flop is currently in the state "1", junction J5 opens and the fluxoid leaves the circuit without disturbing the state of the Flip-Flop. The same is true for the antifluxoid.

EXPERIMENTAL SETUP

The chip was installed on a 24 contact probe and placed in a transport helium dewar. Temperature was stabilized by a Temperature Controller (Lake Shore).. Measurements were carried out using an automated testing setup which had been developed at Stony Brook. Its hardware part is an advanced version of the system developed earlier at NIST. The setup consists of three main parts: a cryoprobe with passive LF filters located in a transport dewar, a set of 48 ADCs and 48 DACs, and IBM PC running *Octopus* software. *Octopus* was used for all low-frequency analog and digital experiments with High-Tc RSFQ RS Flip-Flop. *Octopus* is a TCL interpreter extended to have low-level access to the buses and system timer. It can display real-time analog data, acquire I-V curves and perform various kinds of digital testing. One of the elementary operation used for testing the high-Tc RSFQ RS Flip-Flop is sending a test pattern to the tested circuit and verifying its response.

EXPERIMENTAL DATA

The experimental procedure for testing the RSFQ RS Flip Flop was the following.

1. The operating temperature 26 K was chosen so that the critical current of the SQUID was 50 μA. At this critical current the maximum voltage modulation depth was 12 μV.

2. Transmission line was biased by currents I2L(R), I3L(R), I4L(R) equal to 0.1 mA each. This value corresponds to approximately half the value of critical current of each junction in the transmission line.

3. The SFQ/DC converter was biased at 65 μA and magnetic currents IB5L-IB5L were chosen to have maximum voltage difference between state "0" and "1".

4. The current IL was applied and voltage V_{sq} on the SFQ/DC converter was measured while increasing IL. At some value of IL there appeared a jump in V_{sq} (Fig. 4a) which corresponds to fluxoid entering the main loop ("record" or "flip"). Stability of state "1" can be checked by once more increasing IL to make sure that there are no other states (Fig. 4b).

5. To switch the device from "1" to "0" current IR was applied and at some value there is a jump in V_{sq} from "1" back to "0" state ("erase" or "flop", Fig. 4c). Fig. 4d shows a proof that the device is still in state "0".

To eliminate direct influence of the currents IL and IR on the SFQ/DC converter and Flip-Flop we applied an additional small differential current between IB5L and IB5R proportional to the currents IL or IR to compensate leakage current from the input. The coefficient of proportionality gives us an exact value of the leakage current which was approximately 5% of the input currents IL and IR. This procedure fixes a set point of SFQ/DC converter during all measurements. This fact completely rules out the possibility of switching SQUIDs due to the leakage current.

Operation of the flip-flop is demonsrated in Figure 5. A sequence of digital double current pulses is applied to IL and IR and switches the flip-flop to states "0" and "1" respectively. It can be seen that the first pulse from IL sets the flip-flop ("1") and the second IL pulse does not change the state of the flip-flop. The pulse IR resets the flip-flop ("0"), etc. The noise is characterized by the width of the corresponding voltages V_{sq}.

Peter A. Rosenthal, Senior Physicist

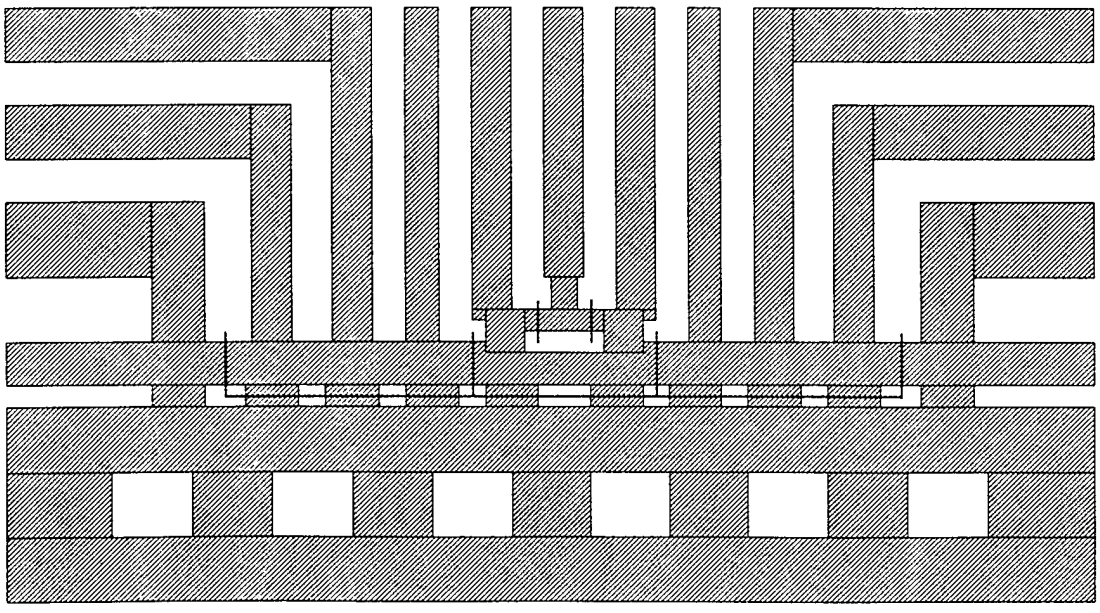

Figure 1. Single-layer layout of the RSFQ circuit. Minimum line width is 2 μm. Solid lines across the bridges denote e-beam junctions.

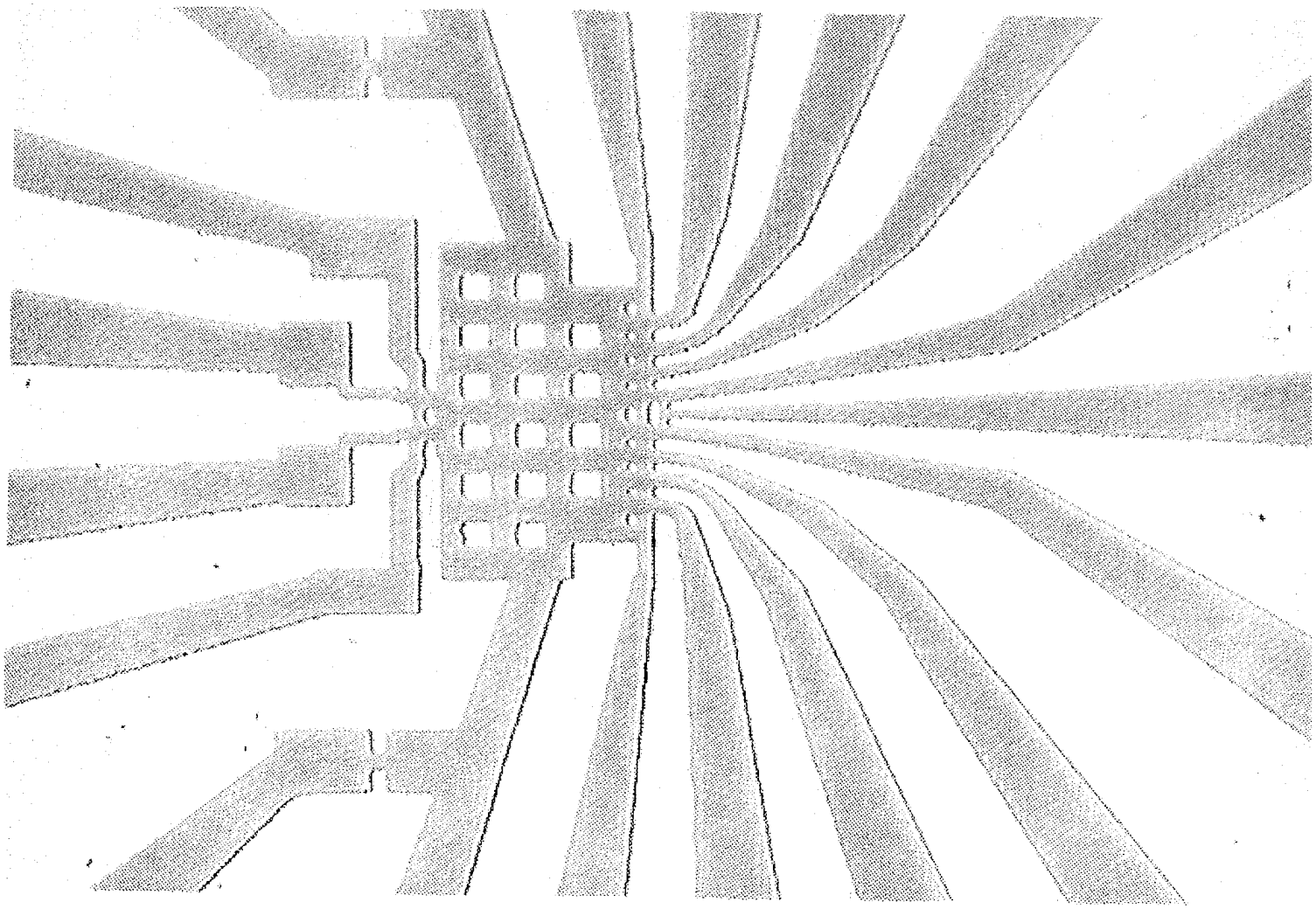

Figure 2. Optical Photograph of the RSFQ Flip-Flop.

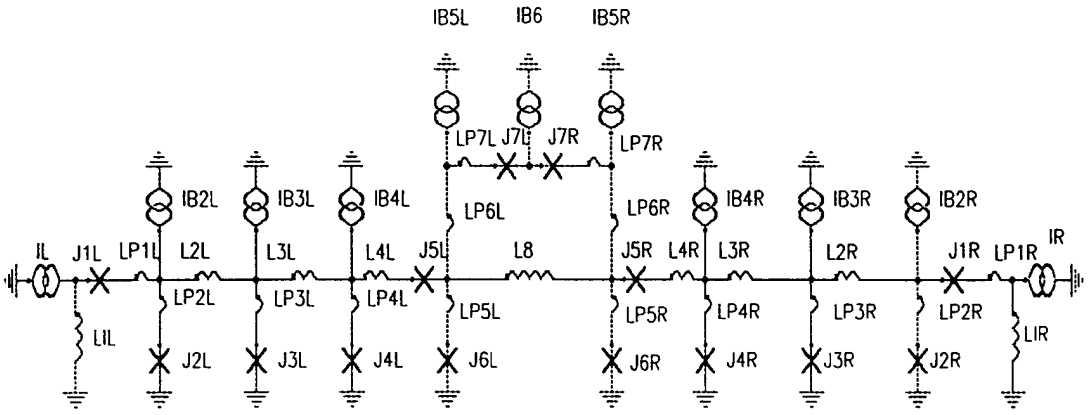

Figure 3. Equivalent circuit of an RSFQ structure comprising two input DC/SFQ converters, two JTLs, RS flip-flop and SFQ/DC converter.

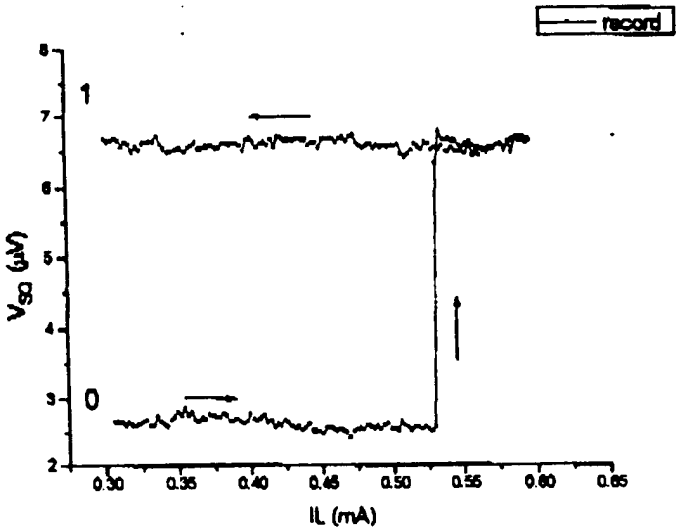

Fig. 4a

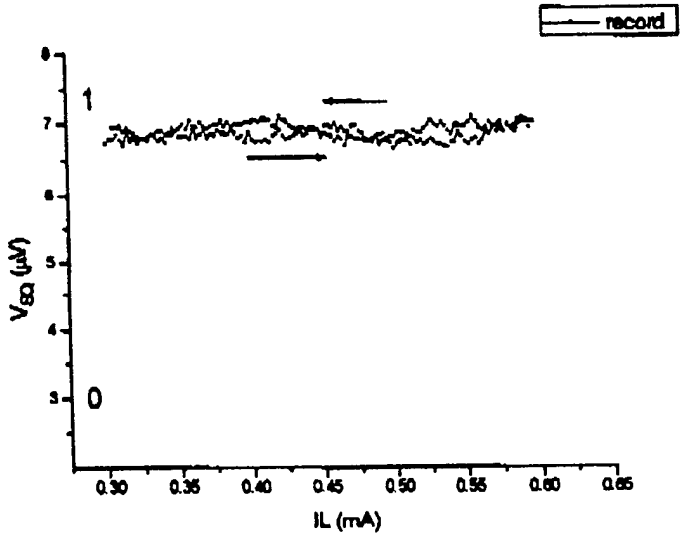

Fig. 4b

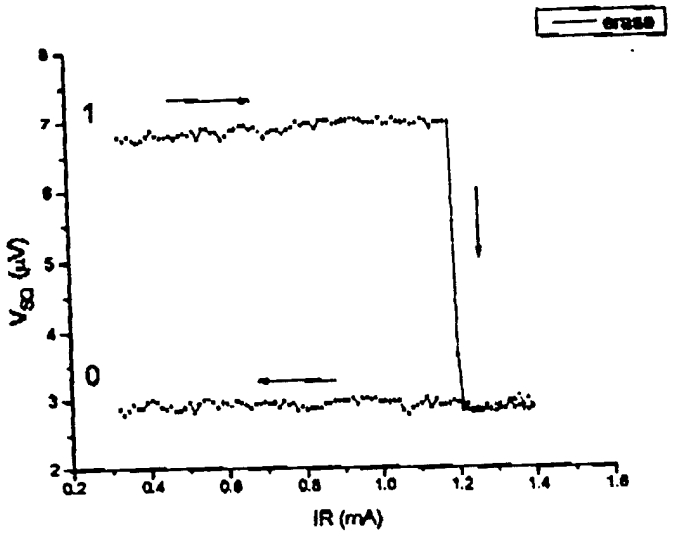

Fig. 4c

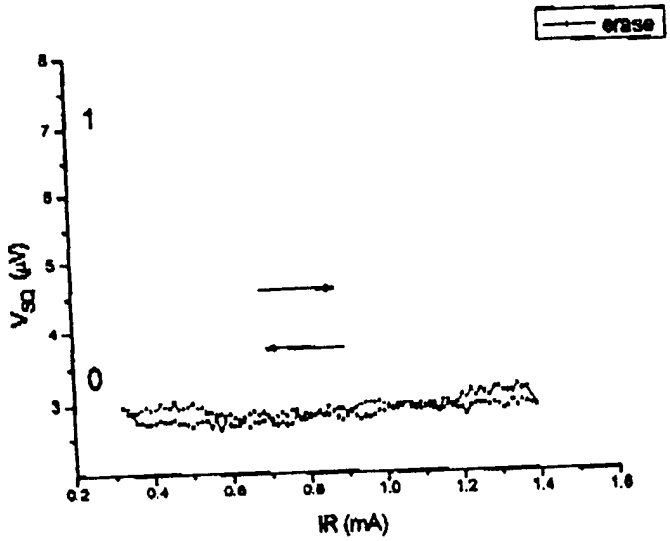

Fig. 4d

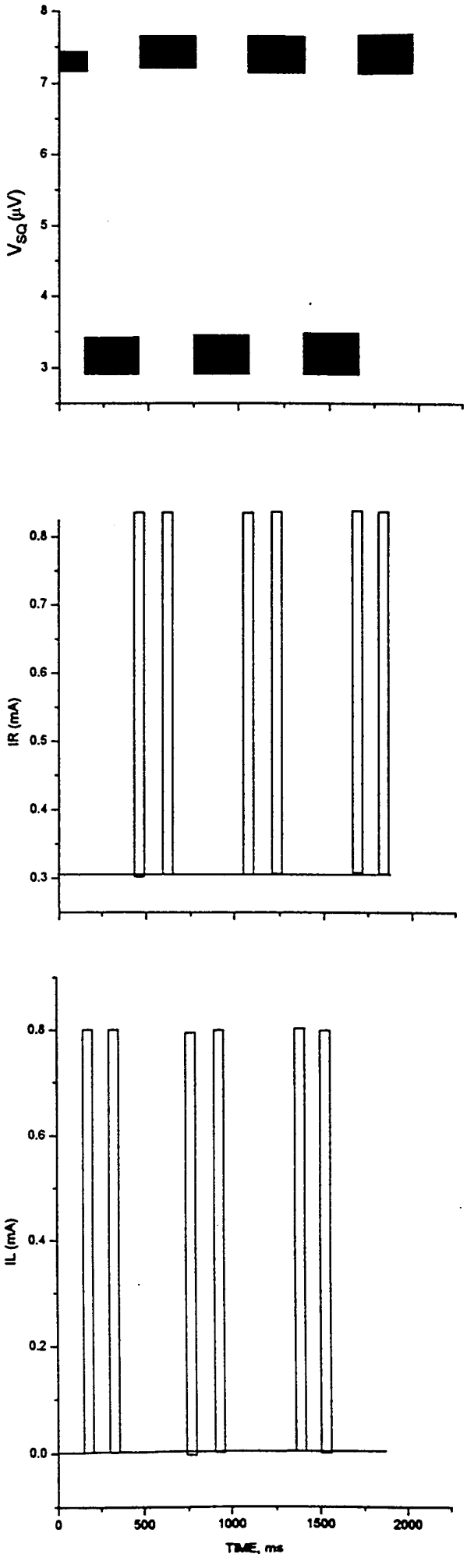
8
7
6
5
4
3
V_{SQ} (μV)
0.8
0.7
0.6
0.5
0.4
0.3
IR (mA)
0.8
0.6
0.4
0.2
0.0
IL (mA)
0
500
1000
1500
2000
TIME, ms

Fig. 5